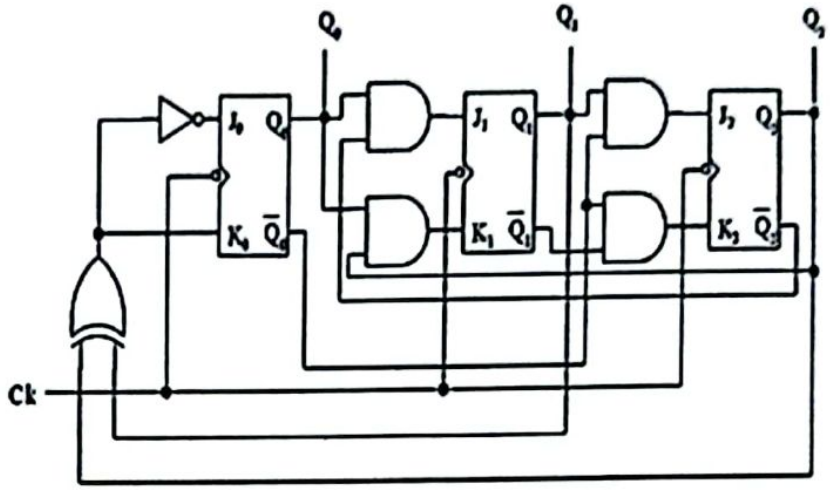
May, 11 , 2024

Final exam

Exercise 1 : (8 pts)

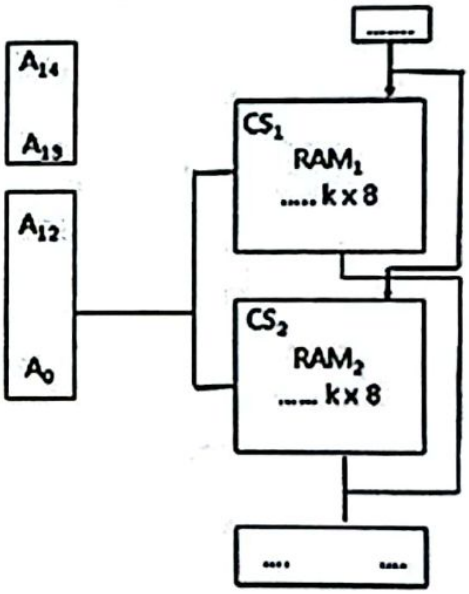
Consider the following sequential circuit:



1. Give the expressions for the flip-flop inputs.(1,5pts)
2. Draw up the characteristic table of the circuit (Q2 is the output of the most significant flip-flop) (2pts)
3. What does this circuit do? Justify.0.5pt
4. Remake the circuit using T flip-flops. (Simplified equations + circuit). .(1,5 +1,5+1)

Exercise 2 : (6 pts)

1. Complete the following memory diagram with the missing values. (1,5pts)
In fact RAM1 consists of two identical blocks whose word size is 8 bits and RAM2 consists of two identical blocks whose word size is 4 bits.
2. Give the addressing range of each block. (1,5pts)
3. Give the complete diagram with the blocks that make up the two RAMs. (1,5pts)
4. Is this machine expandable with blocks of the same size as RAM1 in question 1 (justify). If yes, how many blocks can be added and what is the addressing range of each block. (1,5pts)



Exercise 3 : (6 pts)

1. Replace the question marks with the appropriate expressions to result in the execution of the sequence of instructions as follows :2pts

   a. ? ?, IND → (Acc) = 40
   b. ? ?, XR1 → (Acc) = 25
   c. ? ?, IMM → (Acc) = 5
   d. ? ?, D → (Acc) = 30

ACC	20
XR1	0003

ADDRESS	CONTENT
0100	25
0200	2
FF20	15
FFAB	0200

2. Write a program that calculates the volume of a cylinder of radius R and height H and displays it on the screen knowing that $V = PI*R^2*H$. The R and H values are read as input. The value of PI is considered to be the constant PI=3.14. (2,5pts)
3. We want to add to the previous program the calculation and display of the surface area of the cylinder, knowing that $S = 2*PI*R*H$, add the minimum of instructions. (1,5pts)

Good luck!

FI (STRM2)
1st year Licence in computer science

May 11 2024

Correction of STRM2 exam

EX01

1) Expression des entrées des bascules:

$$\begin{cases} J_0 = \overline{Q_1 \oplus Q_2} \\ K_0 = Q_1 \oplus Q_2 \end{cases} ; \begin{cases} J_1 = Q_0 \bar{Q}_2 \\ K_1 = \bar{Q}_1 \bar{Q}_0 \end{cases} ; \begin{cases} J_2 = Q_1 \bar{Q}_0 \\ K_2 = \bar{Q}_1 \bar{Q}_0 \end{cases}$$

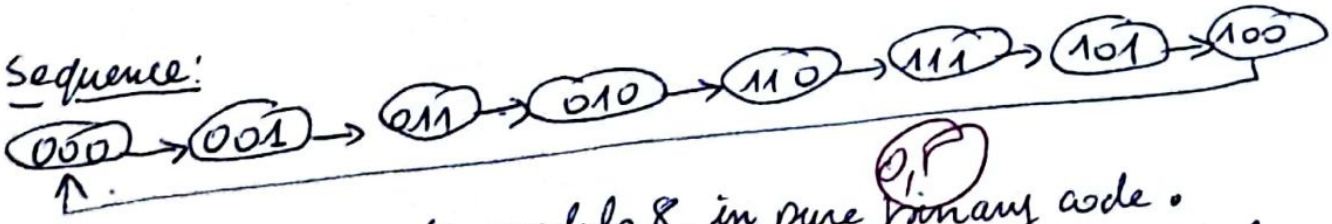
(0,1) (0,1) (0,1)

characteristic table:

Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	1	0	0	1	0	0	0	1
0	0	1	0	0	1	0	1	0	0	1	1
0	1	0	1	0	0	0	0	1	1	1	0
0	1	1	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	0	0	1	0	0	0
1	0	1	0	0	0	1	0	1	1	0	0
1	1	0	1	0	0	0	1	0	1	1	1
1	1	1	0	0	0	1	1	0	1	0	1

(2)

3) Sequence:



(0,5)

It's a random counter modulo 8. in pure binary code.
Also it's a progressive counter modulo 8 in ~~code~~ Gray code.

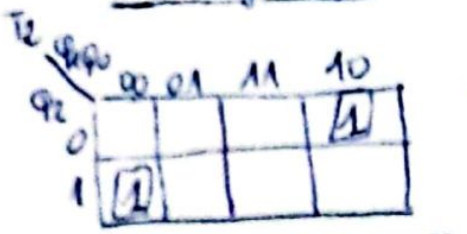
4) realization using T flip-flops.

excitation table:

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	1	0	1	0	0	0	1
1	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1
1	1	0	1	1	1	0	0	1
1	1	1	1	0	1	0	1	0

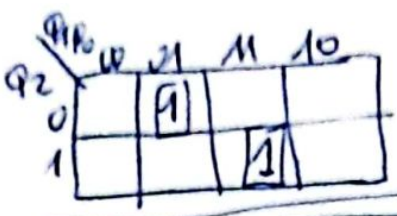
(1,5)

Karnaugh map

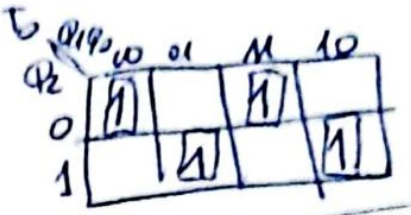


$T_2 = Q_2\bar{Q}_1\bar{Q}_0 + \bar{Q}_2 Q_1 \bar{Q}_0$

$T_2 = \bar{Q}_0 (Q_2 \oplus Q_1)$ 0,5

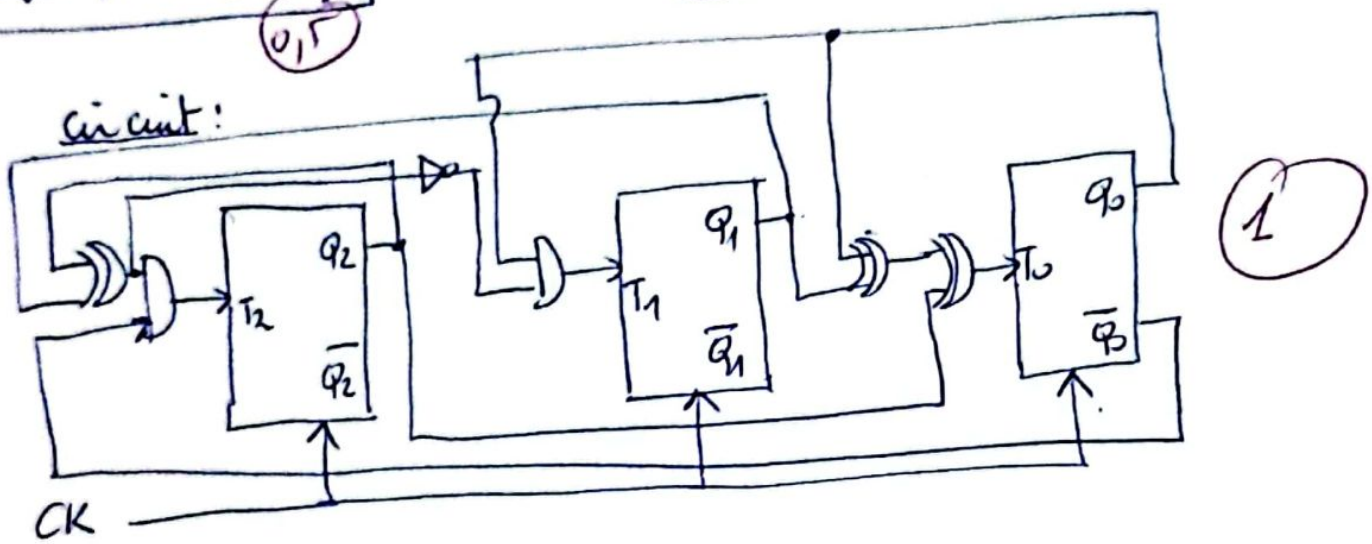


$T_1 = Q_0 (\overline{Q_2 \oplus Q_1})$ 0,5



$T_0 = Q_2 \oplus (Q_1 \oplus Q_0)$ 0,5

circuit:



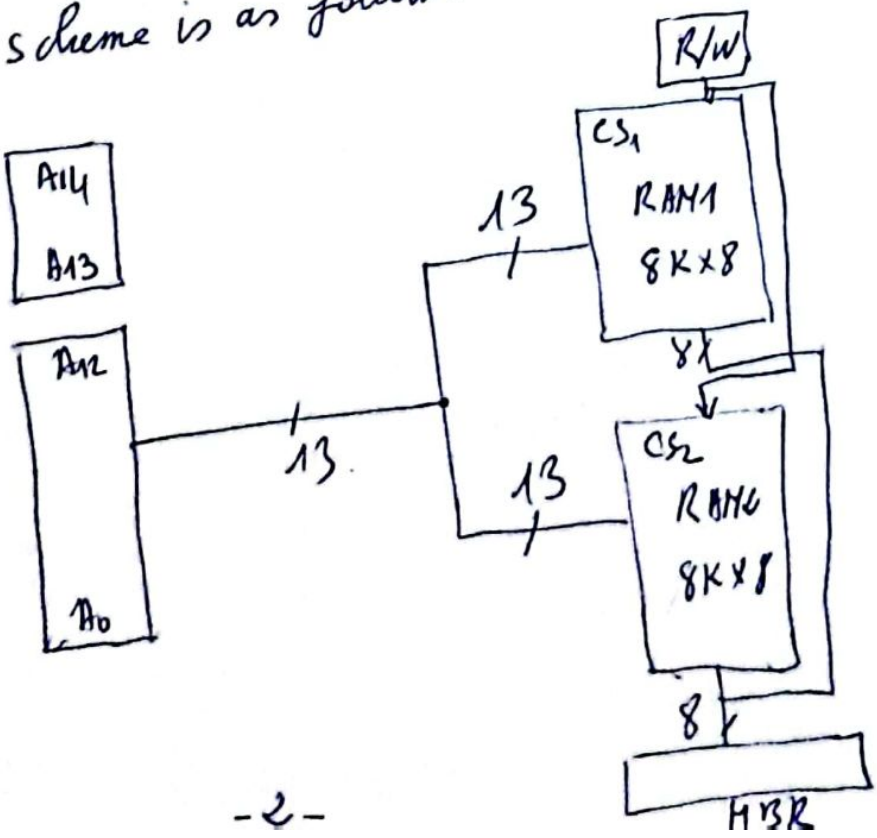
1

Ex02:

RAM1 and RAM2 memories are addressable with 13 bits each

⇒ we have 2^{13} words $= 2^3 \cdot 2^{10} = 8K$ words. So the words in RAM1 and RAM2 are on 8 bits ⇒ MBR = 8 bits

So, the scheme is as follow:



1,1

2) RAM1 . Two identical blocks with word size = 8 bit

so, $\frac{8K \times 8}{2} = 4K \times 8 = (RAM_1)_1 = (RAM_1)_2$.

to address each block we need n to address lines / $2^n = 4K$

$\Rightarrow 2^n = 2^{12} \Rightarrow n = 12$ lins

RAM2 : Two ~~blocks~~, identical blocks with word size is 4 bits, so we need $2 \times (8K \times 4)$ placed in series to have $8K \times 8$.

to address these 2 blocks it's necessary n address lins

/ $2^n = 8K \Rightarrow n = 13$ lins

1,5

Addressing range of each block :

A_{14}	A_{13}	A_{12}	A_{11}	...	A_0	
0	0	0	0	0 ...	0	$(RAM_1)_1$
					1	
0	0	0	1	1 ...	0	$(RAM_1)_2$
0	0	1	0	0 ...	1	
0	0	1	1	1 ...	0	$(RAM_2)_1$ + $(RAM_2)_2$
0	1	0	0	0 ...	1	
0	1	0	1	1 ...	0	
1	0	0	0	0 ...	0	block1 added [4000, 5FFF]
1	0	1	1	1 ...	0	
1	1	0	0	0 ...	1	block2 added [6000, 7FFF]
1	1	1	1	1 ...	1	

Addressing range of $(RAM_1)_1$:

$[0000, 0FFF]$

Addressing range of $(RAM_1)_2$:

$[1000, 1FFF]$

Addressing range of $(RAM_2)_1 + (RAM_2)_2$:

$[2000, 3FFF]$

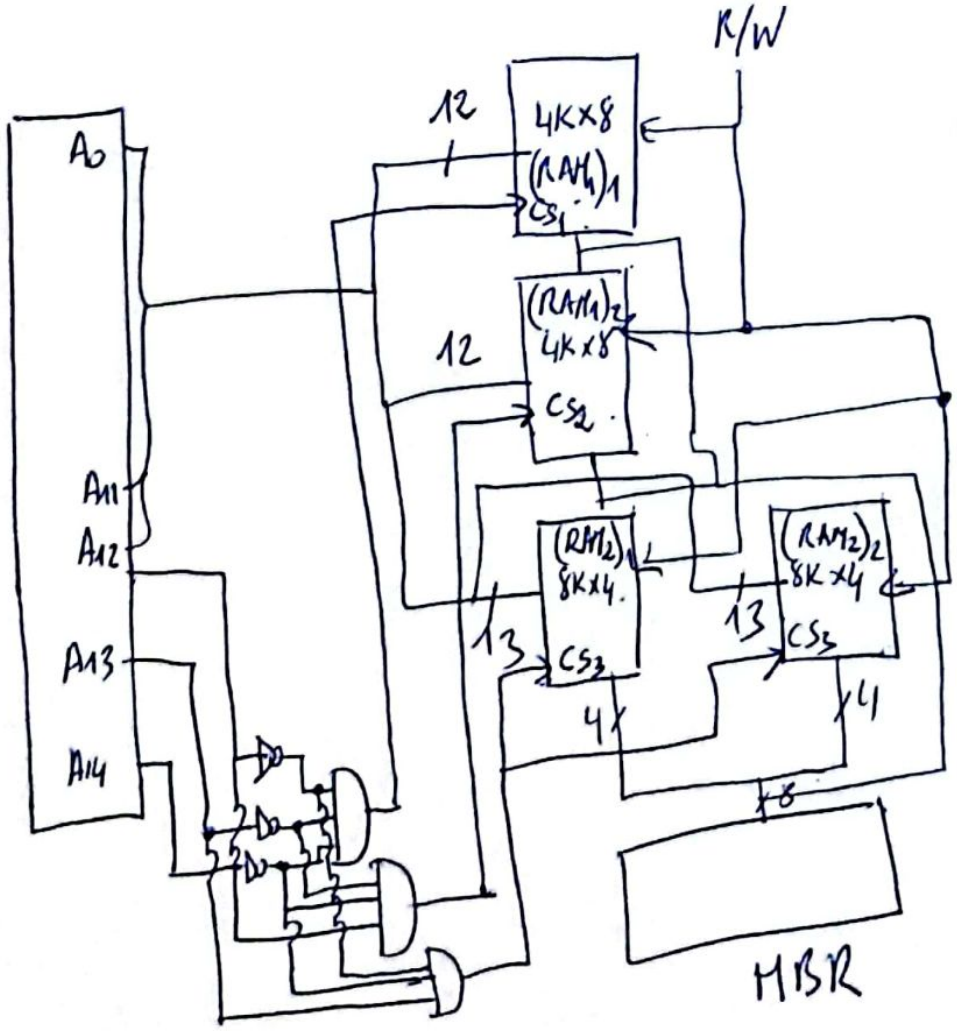
3) Complete diagram:

~~chip select of RAMs~~ (see addressing range)

~~CS~~ $(RAM_1)_1 \Rightarrow CS_1 = \overline{A_{14}}\,\overline{A_{13}}\,\overline{A_{12}}$

$(RAM_1)_2 \Rightarrow CS_2 = \overline{A_{14}}\,\overline{A_{13}}\,A_{12}$

$(RAM_2)_1 + (RAM_2)_2 \Rightarrow CS_3 = \overline{A_{14}}\,A_{13}\overline{A_{12}}$



1,5

4) Yes this machine is expandable

Total capacity of the machine is 2^{15} words = 32K words

we have used only 16 K words, so we can add

16K. With block of 8K we can add 2 blocks. RAM1

Addressing range (see previous addressing range) (1,5)

block1 : [4000, 5FFF]

block2 : [6000, 7FFF]

Exo3 :

1) a). MUL (200), IND (Acc)=40 (0,5) (Acc ← Acc x (200)
Acc ← 20 x 2 = 40)

b) LOAD X, XR1 Acc = 25

X+XR1 = 0100 ⇒ X = $(0100-3)_{16}$ = 00FD

So, LOAD 00FD, XR1 : Acc ← (00FD+3) = 25. (0,5)

other solution

SUB FF1D, XR1 : Acc ← Acc - (FF1D+(XR1)) = 40-15
(FF20) = 25

c) Div 5, IMM Acc = 5 (Acc ← Acc/5 = 25/5 = 5) (0,5)

d) ADD (0100), D : Acc = 30 (0,5) (Acc ← Acc+(100)
Acc ← 5+25 = 30

2) $V = PI \cdot R^2 \cdot H$

READ	Acc ← h.
STORE H, D.	(H) ← Acc
READ	Acc ← r.
STORE R, D	(R) ← r.
MUL R, D.	Acc ← Acc * (R) = R^2.
MUL H, D	Acc ← Acc * (H) = $R^2 \times H$
MUL PI, IMM.	Acc ← Acc * PI = $R^2 \times H \times PI$
STORE V, D.	V ← (Acc) = V ← $R^2 \times H \times PI$
WRITE	

2,5

3) $S = 2 \cdot PI \times R \times H$.

we add the following instruction:

1,5

MUL 2, IMM. :	Acc ← Acc * 2 = $R^2 \times H \times PI \times 2$
DIV R, D.	Acc ← Acc/(R) = $\frac{R^2 \times H \times PI \times 2}{R}$ = $R \times H \times PI \times 2$
STORE S, D.	S ← (Acc) = 2PIRH.